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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,415	03/28/2001	Yehiel Gotkis	LAM2P246	3672

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MARTINE & PENILLA, LLP
710 LAKEWAY DRIVE
SUITE 170
SUNNYVALE, CA 94085

EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/821,415	GOTKIS ET AL.	
	Examiner	Art Unit	
	Hung K. Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,8 and 26-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,8 and 26-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1 A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 05/03/04 has been entered. An action on the RCE follows.

Claim Objections

2. Claims 8, 26, 27, 29-33 and 35 are objected to because of the following informalities: In claims 8, 26, 27, 29-33 and 35, line 1, "A" should be changed to "The" for clarity. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 8 and 26-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekiguchi (PN 6,333,255, of record) in view of Ahn et al. (PN 6,277,728, of record).

Sekiguchi discloses, as shown in Figures 4(c) and 5(c), a semiconductor device comprising,

a substrate (1) having transistor devices [Col. 12, lines 55-61] and a passivation layer (lower 19b) disposed over a dielectric layer (lowermost portion of 22) that is defined over the transistor devices;

a plurality of copper interconnect metallization lines and conductive vias (17, two outside lines) defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a low-k dielectric material (22) [Col. 12, lines 61-65, Col. 13, lines 5-13 and 24-39, and Col. 17, lines 1-10];

a plurality of supporting stubs (17, two inside lines), each of the plurality of supporting stubs configured to form a supporting column that is disposed over a surface of the passivation layer and extends through the plurality of interconnect levels of the semiconductor device, the plurality of supporting stubs is not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias. Note that it is inherent that the two inside lines provide support structure.

Sekiguchi does not disclose the low-k dielectric material is a porous dielectric material. However, Ahn et al. discloses the plurality of copper interconnect metallization lines and conductive vias (48,54,70) isolated from each other by low-k dielectric material (56) including a porous dielectric material. Note Figures 1-12 and Table of Ahn et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the low-k dielectric material of Sekiguchi by a porous dielectric material, such as taught by Ahn et

al. because a porous dielectric material is commonly used as the interlayer dielectric material and it helps to reduce the coupling capacitance between the interconnects.

With regard to claim 30, Sekiguchi and Ahn et al. disclose the plurality of supporting stubs is not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias [see Figures 4(c) and 5(c)].

With regard to claims 8 and 31, Sekiguchi and Ahn et al. disclose the device further comprising a passivation-capping layer (upper 19b) defined over a topmost layer of the copper interconnect metallization lines and conductive vias [see Figures 4(c) and 5(c)].

With regard to claims 26 and 32, Sekiguchi and Ahn et al. disclose the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures [see Figures 4(c) and 5(c)].

With regard to claims 27 and 33, Sekiguchi and Ahn et al. disclose the plurality of supporting stubs further support a passivation layer (19b) [see Figures 4(c) and 5(c)].

4. Claims 6, 8 and 26-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunikiyo (PN 6,717,267) in view of Ahn et al. (PN 6,277,728, of record).
Kunikiyo discloses, as shown in Figures 6-36, a semiconductor device comprising,

a substrate (1) having transistor devices (50) and a passivation layer (5) disposed over a dielectric layer (4) that is defined over the transistor devices;

a plurality of copper interconnect metallization lines and conductive vias (20a-20c,19a-19d,29b-29c,) defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a dielectric material (10,23);

a plurality of supporting stubs (21a-21b,22a-22b), each of the plurality of supporting stubs configured to form a supporting column that is disposed over a surface of the passivation layer and extends through the plurality of interconnect levels of the semiconductor device, the plurality of supporting stubs is not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

Kunikiyo does not disclose the dielectric material is a porous dielectric material. However, Ahn et al. discloses the plurality of copper interconnect metallization lines and conductive vias (48,54,70) isolated from each other by dielectric material (56) including a porous dielectric material. Note Figures 1-12 and Table of Ahn et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dielectric material of Sekiguchi by a porous dielectric material, such as taught by Ahn et al. because a porous dielectric material is commonly used as the interlayer dielectric material and it helps to reduce the coupling capacitance between the interconnects.

With regard to claim 30, Kunikiyo and Ahn et al. disclose the plurality of supporting stubs (dummy) is not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

With regard to claims 8 and 31, Kunikiyo and Ahn et al. disclose the device further comprising a passivation-capping layer (27) defined over a topmost layer of the copper interconnect metallization lines and conductive vias [See Figures 7-36].

With regard to claims 26 and 32, Kunikiyo and Ahn et al. disclose the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures [see Figures 6-36].

With regard to claims 27 and 33, Kunikiyo and Ahn et al. disclose the plurality of supporting stubs further support a passivation layer (27) [see Figures 6-36].

With regard to claim 34, Kunikiyo and Ahn et al. disclose the dielectric layer is non-porous dielectric [SiOF, Col. 11, lines 20-23]

Response to Arguments

5. Applicant's arguments filed 05/03/04 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., each of the supporting stubs forms a supporting column that is disposed over the passivation layer, and not the source/drain region, and do not have any electrical functionality) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It is argued, at pages 7 and 8 of the Remarks, that Sekiguchi and Ahn et al. failed to teach forming of an ILD layer over the substrate surface and the transistor devices, and a passivation layer formed over the ILD layer. This argument is not convincing because, Sekiguchi discloses, as shown in Figures 4(c) and 5(c), an ILD layer (lower portion 22) is formed over the substrate surface and the transistor devices, and a passivation layer (lowever layer 19b) is formed over the ILD layer.

It is argued, at page 7 of the Remarks, that modified multilevel structure of Sekiguchi would have a higher dielectric constant than the semiconductor of the claimed invention wherein the interconnect metallization lines and conductive vias are isolated by porous dielectric material since the modified multilevel structure would still include all the upper and lower silicon dioxide or silicon nitride insulators in addition to the porous low-K dielectric formed around the interconnect lines, trenches, and vias. This argument is not convincing because the claimed

language does not specifically state whether only the porous dielectric material is between the lines and vias.

6. Applicant's arguments with respect to claims 6, 28 and 34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

June 21, 2004

Hung Vu

Patent Examiner